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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/263,766	03/05/1999	TSUYOSHI TOMITA	P8075-9006	2214

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EXAMINER	
BURD, KEVIN MICHAEL	
ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 10/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/263,766	TOMITA, TSUYOSHI	
	Examiner	Art Unit	
	Kevin M. Burd	2631	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-15* is/are allowed.

6)☒ Claim(s) *16-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This office action, in response to the amendment and the request for continued examination filed 9/16/2004, is a final office action.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/16/2004 has been entered.

Response to Arguments

3. Applicant's arguments filed 9/16/2004 have been fully considered but they are not persuasive. Applicant has amended claim 16 so that the loop control circuit includes an independent circuit that is independent of the decision circuit and performs a calculation with the feedback signal and the filtered signal. This new limitation is stated below. Applicant has added new limitations to claim 17 as well. These new limitations are addressed below. New claims 18 and 19 have been added and are addressed below.

Claim 18 is substantially the same as claim 16 prior to the amendment of 9/16/2004. The previous rejection of claim 16 is applied to new claim 18.

All claims are drawn to the same invention claimed in the earlier application and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the earlier application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 16-19 are rejected under 35 U.S.C. 102(a) as being anticipated by the instant application's disclosed prior art.

Regarding claim 16, the instant application's disclosed prior art, specifically figure 1, discloses a signal processing circuit. Element 12 is the decision feedback equalizer (page 1, lines 10-15). The equalizer waveform equalizes a digital signal (RD) in accordance with a clock signal (CLK).

A timing recovery phase locked loop (element 16) is disclosed for generating a clock signal. The clock signal will have substantially the same phase as the digital signal once equalization has been achieved. Element 12 comprises a prefilter 21, a decision circuit connected to the prefilter 22, a shift register 24 connected to the decision circuit, a feedback filter 25 and a loop control circuit 17 which monitors the output data signal and controls the switches. The loop control circuit 17 is an independent circuit that is independent of the decision circuit 22. The loop filter control circuit performs a

calculation by receiving the DATA signal. The loop control circuit 17 determines the configuration of switches 27-29, thereby controlling a feedback loop formed by the shift register, the feedback filter and the independent loop control circuit as shown in figure 1.

Regarding claim 17, the instant application's disclosed prior art, specifically figure 1, discloses a signal processing circuit. Element 12 is the decision feedback equalizer (page 1, lines 10-15). The equalizer waveform equalizes a digital signal (RD) in accordance with a clock signal (CLK).

A timing recovery phase locked loop (element 16) is disclosed for generating a clock signal. The clock signal will have substantially the same phase as the digital signal once equalization has been achieved. Element 12 comprises a prefilter 21, a decision circuit connected to the prefilter 22, a shift register 24 connected to the decision circuit, a feedback filter 25 and a loop control circuit 17 which monitors the output data signal and controls the switches. The feedback signal is the same as signal DATA which is a waveform equalized digital signal. A loop is generated using the calculation signal from decision circuit 22 and the DATA signal as shown in figure 1.

Regarding claim 18, the instant application's disclosed prior art, specifically figure 1, discloses a signal processing circuit. Element 12 is the decision feedback equalizer (page 1, lines 10-15). The equalizer waveform equalizes a digital signal (RD) in accordance with a clock signal (CLK).

A timing recovery phase locked loop (element 16) is disclosed for generating a clock signal. The clock signal will have substantially the same phase as the digital signal once equalization has been achieved. Element 12 comprises a prefilter 21, a decision

circuit connected to the prefilter 22, a shift register 24 connected to the decision circuit, a feedback filter 25 and a loop control circuit 17 which monitors the output data signal and controls the switches.

Regarding claim 19, the instant application's disclosed prior art, specifically figure 1, discloses a signal processing circuit. Element 12 is the decision feedback equalizer (page 1, lines 10-15). The equalizer waveform equalizes a digital signal (RD) in accordance with a clock signal (CLK).

A timing recovery phase locked loop (element 16) is disclosed for generating a clock signal. The clock signal will have substantially the same phase as the digital signal once equalization has been achieved. Element 12 comprises a prefilter 21, a decision circuit connected to the prefilter 22 conducting a first calculation, a shift register 24 connected to the decision circuit, a feedback filter 25 and a loop control circuit 17 which monitors the output data signal and controls the switches. The loop filter control circuit 17 performs a second calculation by receiving the DATA signal. The loop control circuit 17 determines the configuration of switches 27-29, thereby controlling a feedback loop formed by the shift register, the feedback filter and the independent loop control circuit as shown in figure 1.

Conclusion

5. This is an RCE of applicant's earlier Application No. 09/263,766. All claims are drawn to the same invention claimed in the earlier application and could have been finally rejected on the grounds and art of record in the next Office action if they had

been entered in the earlier application. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action in this case. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no, however, event will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin M. Burd whose telephone number is (571) 272-3008. The examiner can normally be reached on Monday - Thursday 9 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kevin M. Burd
10/9/2004

KEVIN BURD
PATENT EXAMINER